Integrated Circuit Systems, Inc.

ICS86962I-01

LOW SKEW, 1-TO-18 LVCMOS/LVTTL ZERO DELAY BUFFER

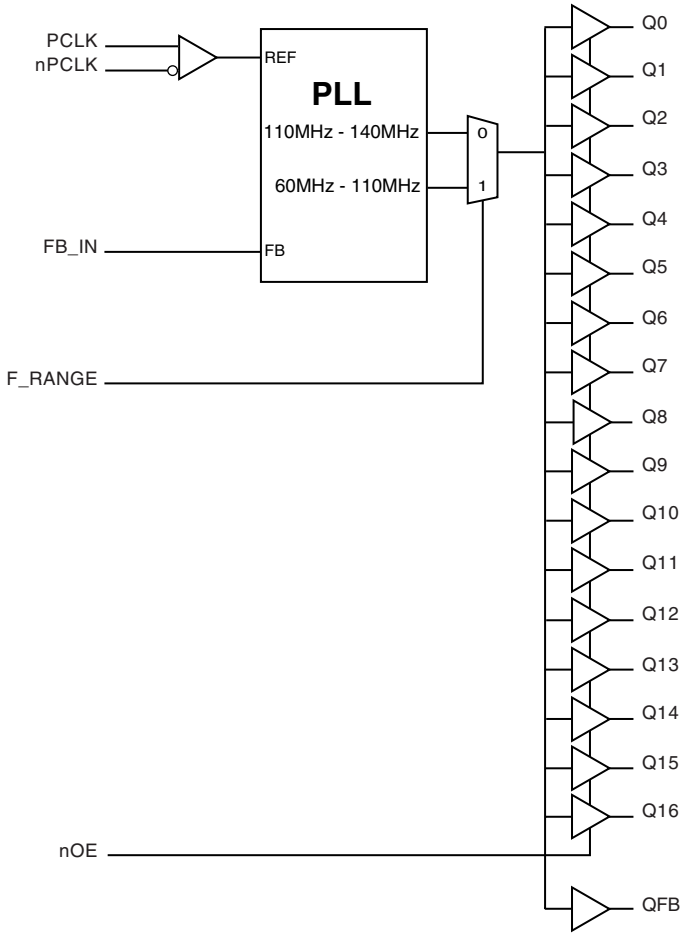
GENERAL DESCRIPTION

The ICS86962I-01 is a low voltage, low skew LVCMOS/LVTTL Zero Delay Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. With output frequencies up to 140MHz, the ICS86962I-01 is targeted for high performance clock applications. Along with a fully integrated PLL, the ICS86962I-01 contains frequency configurable outputs and an external feedback input for regenerating clocks with "zero delay".

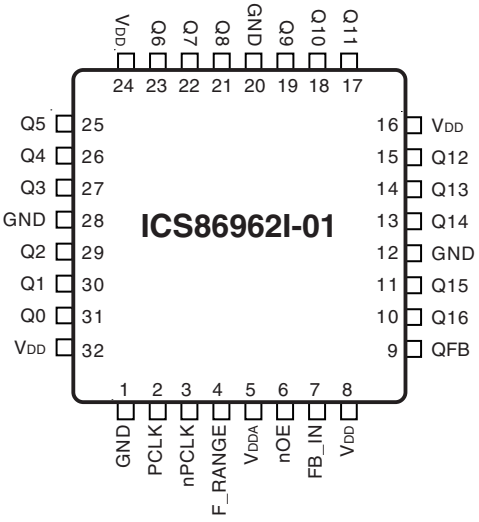
FEATURES

- Fully integrated PLL
- 18 LVCMOS/LVTTL outputs: 17 LVCMOS/LVTTL clock outputs, 1 QFB feedback output. 14Ω typical output impedance
- 1 differential LVPECL clock pair
- PCLK, nPCLK pair supports the following input types: LVPECL, LVDS, CML, SSTL
- Input/Output frequency range: 60MHz to 140MHz
- External feedback for "zero delay" clock regeneration
- Output skew: 210ps (maximum)
- Cycle-to-cycle jitter: 100ps (maximum)
- Period jitter, RMS: 4ps (maximum)
- Full 3.3V or 2.5V supply voltage
- -40°C to 85°C ambient operating temperature
- Pin compatible to MPC961

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body

Y package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 12, 20, 28	GND	Power		Power supply ground.
2	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
3	nPCLK	Input	Pulldown/ Pullup	Inverts differential LVPECL clock input. V_{DD}/2 default when left floating.
4	F_RANGE	Input	Pulldown	PLL frequency range select. LVCMOS / LVTTL interface levels.
5	V_{DDA}	Power		Analog supply pin.
6	nOE	Input	Pulldown	Output enable. Controls the enabling and disabling of outputs. When HIGH, forces Q0:Q16 to a HiZ state. When LOW, enables clock outputs. LVCMOS / LVTTL interface levels.
7	FB_IN	Input	Pulldown	Feedback input to phase detector for generating clocks with "zero delay". LVCMOS / LVTTL interface levels.
8, 16, 24, 32	V_{DD}	Power		Power supply pins.
9	QFB	Output		PLL feedback clock output. LVCMOS / LVTTL interface levels.
10, 11, 13, 14, 15, 17, 18, 19, 21, 22, 23, 25, 26, 27, 29, 30, 31	Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Clock outputs. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
$R_{VCC/2}$	Pullup/Pulldown Resistors			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDA} = 3.465V		7		pF
		V_{DD}, V_{DDA} = 2.625V		8		pF
R_{OUT}	Output Impedance	V_{DD}, V_{DDA} = 3.465V		14		Ω
		V_{DD}, V_{DDA} = 2.625V		18		Ω

TABLE 3A. OUTPUT ENABLE FUNCTION TABLE

Control Input	Outputs
nOE	**Q0:Q16**
0	Enabled
1	HiZ

TABLE 3B. CONTROL INPUT FUNCTION TABLE

Control Input	Input/Output Frequency Range (MHz)	
F_RANGE	**Minimum**	**Maximum**
0	110	140
1	60	110

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	QFB switching @100MHz with 50Ω to $V_{DD}/2$			120	mA
I_{DDA}	Analog Supply Current				15	mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	QFB switching @100MHz with 50Ω to $V_{DD}/2$			110	mA
I_{DDA}	Analog Supply Current				15	mA

TABLE 4C. DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IN}	Input Current		$V_{DD} = V_{IN}$ = 3.465V, $V_{DD} = V_{IN}$ = 2.625V			±120	µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DD} = V_{IN}$ = 3.465V	2.6			V
			$V_{DD} = V_{IN}$ = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DD} = V_{IN}$ = 3.465V, $V_{DD} = V_{IN}$ = 2.625V			0.5	V
V_{PP}	Peak-to-Peak Input Voltage	PCLK, nPCLK		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 2, 3	PCLK, nPCLK		GND + 1.2		V_{DD}	V

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	F_RANGE = 0		110		140	MHz
		F_RANGE = 1		60		110	MHz
f_{MAX}	Output Frequency	F_RANGE = 0		110		140	MHz
		F_RANGE = 1		60		110	MHz
t(Ø)	Static Phase Offset; NOTE 1	PCLK,nPCLK to FB_IN		45		225	ps
*t*sk(o)	Output Skew; NOTE 2, 3					210	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3					100	ps
*t*jit(per)	Period Jitter, RMS					4	ps
t_R, t_F	Output Rise/Fall Time		20% to 80%	400		900	ns
t_{PLZ}, t_{PHZ}	Output Disable Time					5	ns
t_{PZL}, t_{PZH}	Output Enable Time					5	ns
odc	Output Duty Cycle		f ≤ 133MHz	45		55	%

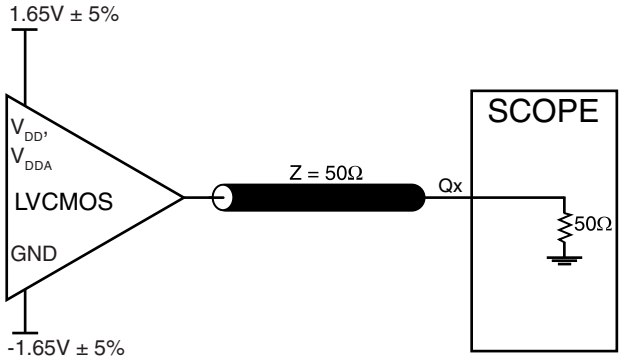
All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Defined as the time difference between the input clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

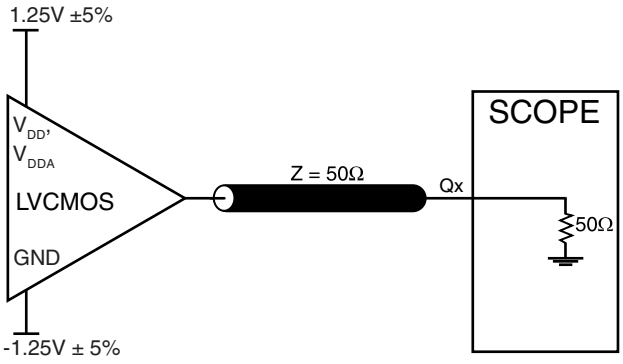
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	F_RANGE = 0		110		140	MHz
		F_RANGE = 1		60		110	MHz
f_{MAX}	Output Frequency	F_RANGE = 0		110		140	MHz
		F_RANGE = 1		60		110	MHz
t(Ø)	Static Phase Offset; NOTE 1	PCLK,nPCLK to FB_IN		0		250	ps
*t*sk(o)	Output Skew; NOTE 2, 3					175	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3					80	ps
*t*jit(per)	Period Jitter, RMS					3	ps
t_R, t_F	Output Rise/Fall Time		20% to 80%	400		900	ns
t_{PLZ}, t_{PHZ}	Output Disable Time					5	ns
t_{PZL}, t_{PZH}	Output Enable Time					5	ns
odc	Output Duty Cycle		f ≤ 133MHz	44		56	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Defined as the time difference between the input clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

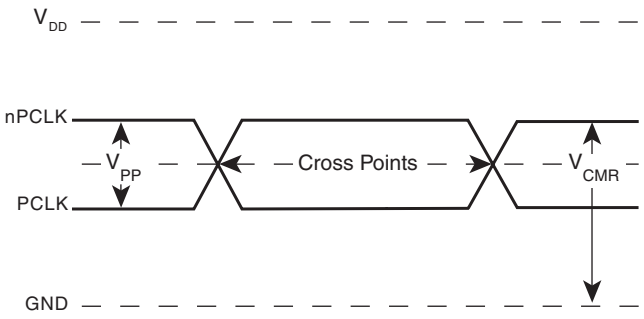
PARAMETER MEASUREMENT INFORMATION



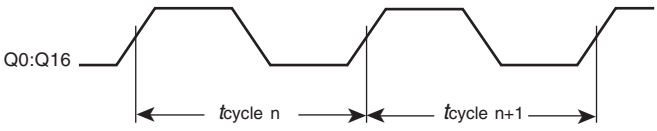
3.3V CORE/ 3.3V OUTPUT LOAD AC TEST CIRCUIT



2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



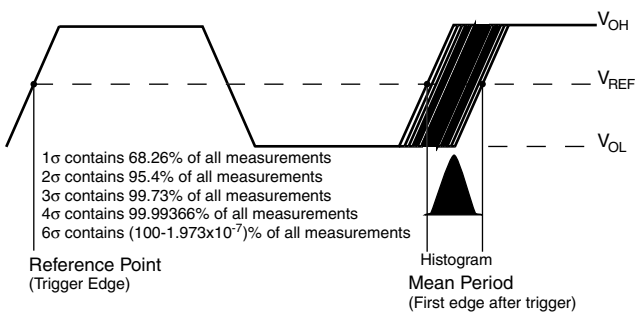
DIFFERENTIAL INPUT LEVEL



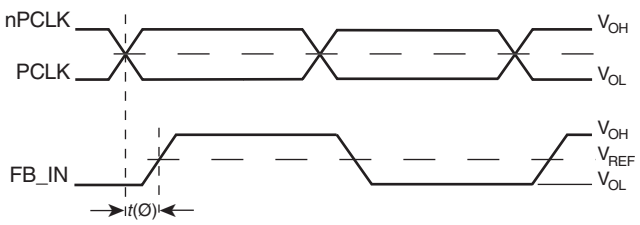
$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

CYCLE-TO-CYCLE JITTER



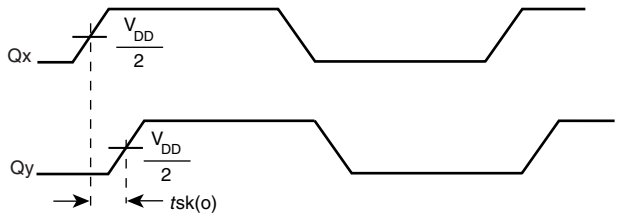
PERIOD JITTER



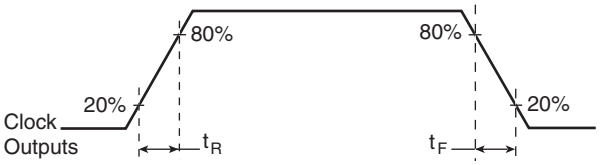
$t(Ø)_{mean}$ = Static Phase Offset

(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

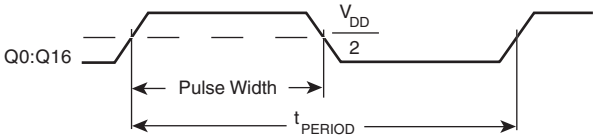
STATIC PHASE OFFSET



OUTPUT SKEW



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

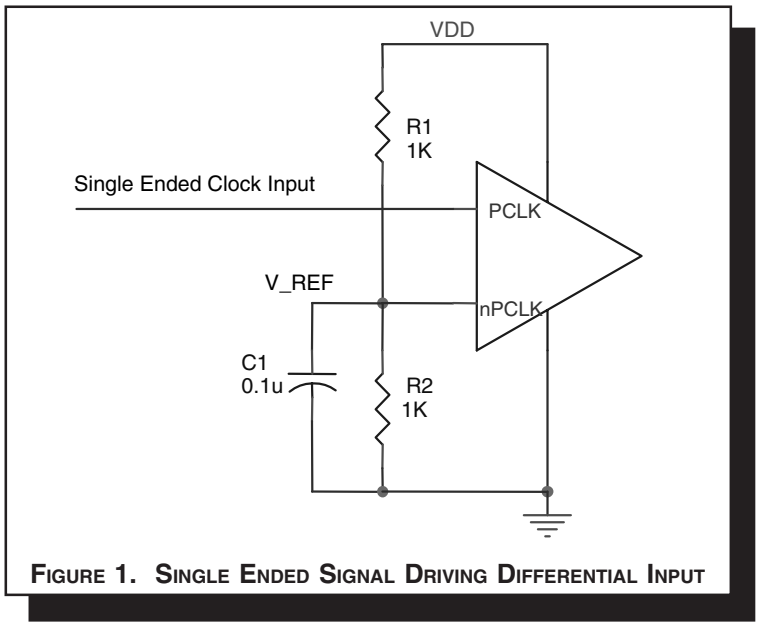


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS86962I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

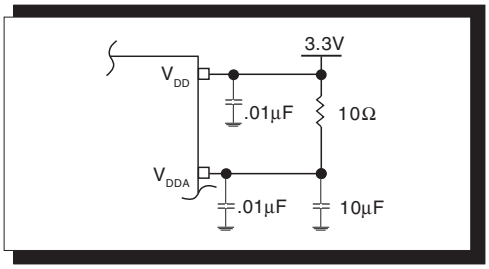


FIGURE 2. POWER SUPPLY FILTERING

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3D* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

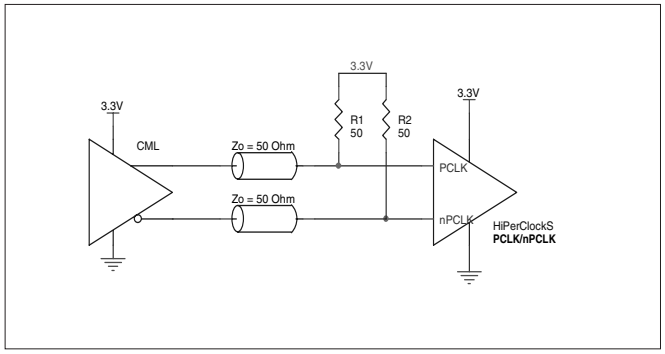


FIGURE 3A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A CML DRIVER

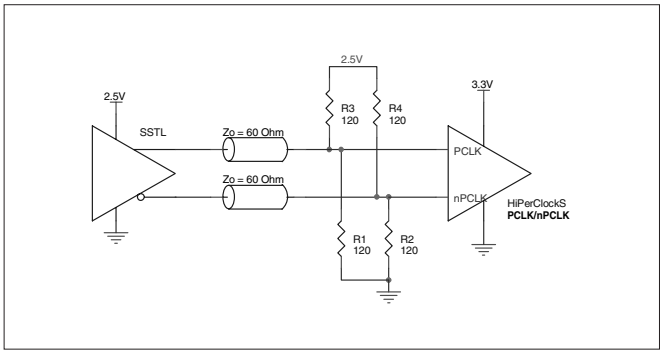


FIGURE 3B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL DRIVER

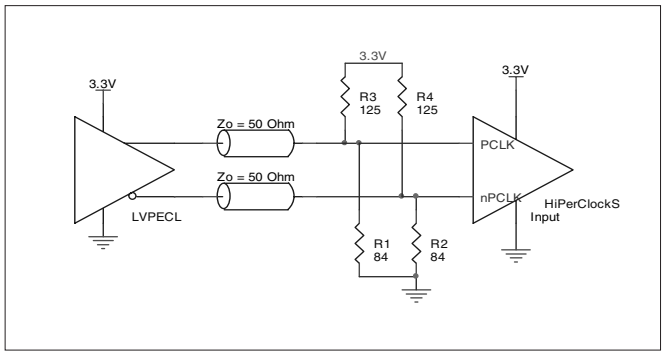


FIGURE 3C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

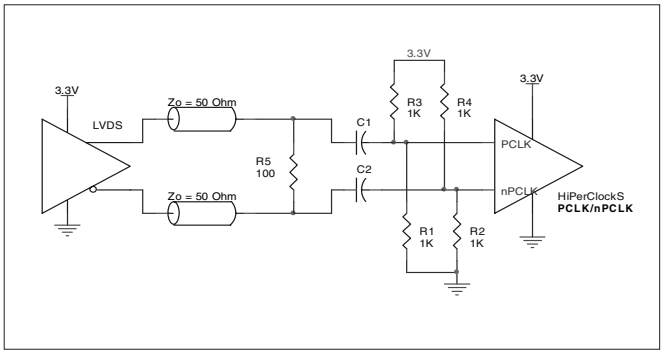


FIGURE 3D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE for 32 Lead LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS86962I-01 is: 1940

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

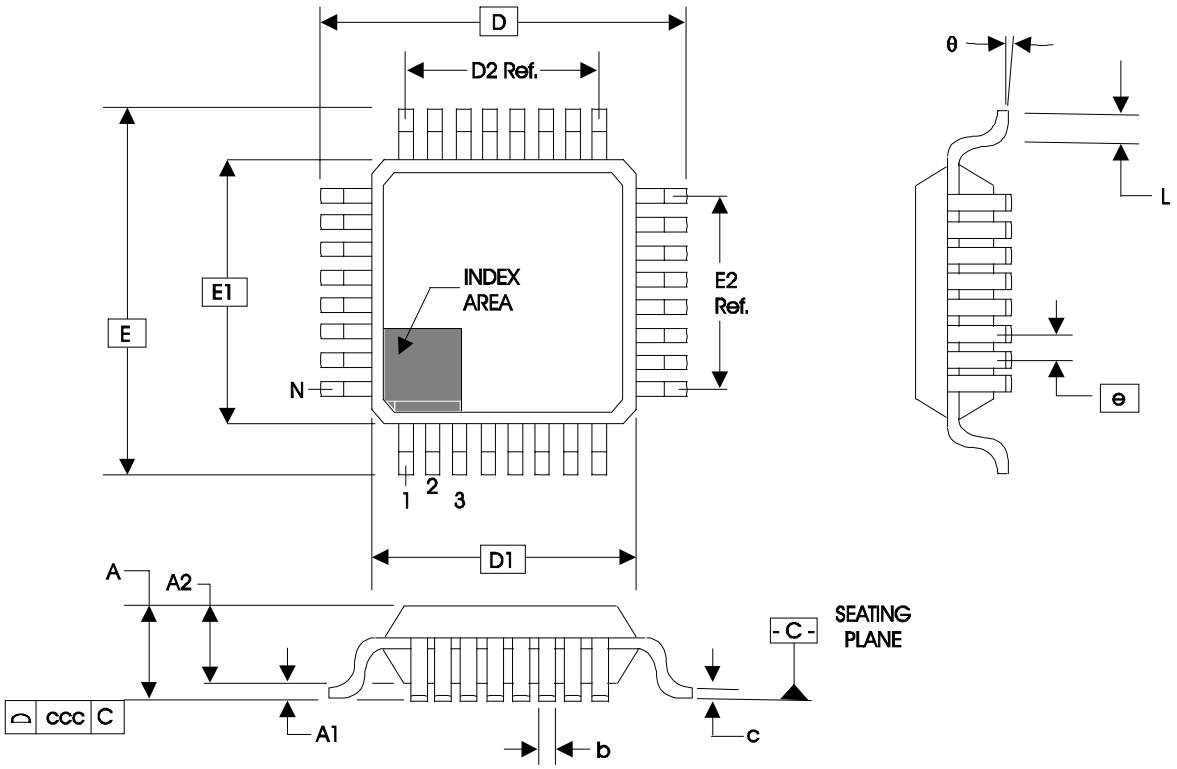


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS86962CYI-01	ICS86962CYI01	32 Lead LQFP	250 per tray	-40°C to 85°C
ICS86962CYI-01T	ICS86962CYI01	32 Lead LQFP on Tape and Reel	1000	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T4B	3	2.5V Power Supply table - corrected the voltage from 3.3V to 2.5V.	10/10/04
A	T8	11	Ordering Information Table - corrected Part/Order Number.	12/14/04